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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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CANTOR COLBURN, LLP
55 GRIFFIN ROAD SOUTH
BLOOMFIELD, CT 06002

EXAMINER	
TRAN, MY CHAU T	
ART UNIT	**PAPER NUMBER**
2629	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	01/23/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/799,823	JANG, HYEON-YONG	
	Examiner	Art Unit	
	MY-CHAU T. TRAN	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 April 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5,9-12,15-18,20 and 21* is/are rejected.

7)☒ Claim(s) *6-8,13,14 and 19* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *4/28/06*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Application and Claims Status

1. Claims 1-21 are currently pending and are under consideration in this Office Action.

Priority

2. Receipt is acknowledged of papers, (i.e. Korean Patent Application No(s). 2003-16041; Filed: March 14, 2003), submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Information Disclosure Statement

3. The information disclosure statement (IDS) filed on 04/28/2006 has been reviewed, and the references that have been considered are initialed as recorded in PTO-1449 form(s).

Claim Rejections - 35 USC § 112

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claim 16 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

a. Claim 16 recites the limitation "*the light source*" in line 1. There is insufficient antecedent basis for this limitation in claim 1 since claim 1 does not recite the structural feature of a '*light source*'. The device of claim 1 claimed the structural features of input

terminals, an oscillator, a controller, and a phase difference detecting unit. Therefore, the limitation of "*the light source*" of claim 16 lack antecedent basis and claim 13 and all its dependent claims are rejected under 35 U.S.C. 112, second paragraph.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

7. Claims 1 and 9 are rejected under 35 U.S.C. 102(b) as being anticipated by Tsunoda et al. (US Patent 5,912,713).

For ***claims 1 and 9***, Tsunoda et al. disclose a display control apparatus that comprises a display control apparatus (ref. #1 of figure 1) and a display panel unit (ref. #3 of figure 1)(see e.g. Abstract; col. 1, lines 41-47; fig. 1). The display control apparatus comprises a PLL circuit (ref. #41 of figure 1). In one embodiment as illustrated in figure 3, the PLL circuit comprises a phase comparator (refers to instant claimed a phase difference detecting unit), a low-pass filter, a voltage-controlled oscillator (refers to instant claimed an oscillator), a selector (refers to instant claimed controller), a hold switch (ref. #20)(refers to instant claimed switch circuit), a frequency divider, the arrow with "HD" label (refers to instant claimed input terminal that receive a horizontal synchronization signal), and the reference arrows #33 and 34 (refers to instant claimed input terminal that receive a control signal externally provided)(see e.g. col. 5, lines 52-61; col. 6, line 45 thru col. 7, line 19). The phase comparator receive the HD signal (refers to instant

claimed horizontal synchronization signal) and the fv signal (refers to instant claimed modulated signal) and detect a phase difference between these two signals and generate an output signal indicating the phase difference, which is sent to the voltage-controlled oscillator wherein the oscillator adjusts the frequency of the f_{out} (refers to instant claimed reference signal) in response to the output signal of the phase comparator so that the HD signal and the fv signal are synchronized with each other (see e.g. col. 5, lines 52-65). The selector modulates the reference signal in response to the control signal and output a modulated signal (see e.g. col. 6, lines 45-61). The frequency divider divide a frequency of the modulated signal provided from the controller to generate a frequency- divided signal (see e.g. col. 6, lines 45-61).

Therefore, the apparatus of Tsunoda et al. do anticipate the instant claimed invention.

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claims 1-5, 9-12, 15, 17, 18, 20, and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tanaka et al. (US Patent 6,011,534) in view of Jefferson (US Patent 6,127,865).

For ***claims 1 and 3***, Tanaka et al. disclose a driving circuit for image display device such as a liquid crystal device (see e.g. Abstract; col. 1, lines 8-15; col. 6, lines 13-23). The driving

circuit includes a PLL circuit (ref. # 2 of fig. 1), which receive signals based on a horizontal synchronizing signal, i.e. HSYN, and a vertical synchronizing signal, i.e. VSYN, of an input composite signal, i.e. CSYN, (refers to instant claimed input terminals)(see e.g. col. 6, lines 13-23; fig. 1). As illustrated by figure 1, PLL circuit comprises a phase comparator (ref. #2a), an integrator (ref. #2b), a voltage control oscillator (ref. #2c) and a divider (ref. #2d)(see e.g. col. 6, line 66 thru col. 7, line 10). The phase comparator compares the phases of the horizontal synchronization signal and the signal from the divider and generates an output signal of which value is determined based on the comparison (see e.g. fig. 1). The integrator generates a voltage signal having a magnitude proportional to an integration of the output signal of the phase comparator (see e.g. col. 7, lines 5-7; fig. 1). The voltage control oscillator generates a signal in response to the output signal of the phase comparator (see e.g. col. 7, lines 1-9; fig. 1).

For ***claim 2***, Tanaka et al. disclose that the signal externally provided includes a signal to control luminance on a screen of the image display device (see e.g. col. 6, lines 24-38 and 55-60).

For ***claims 17 and 18***, Tanaka et al. disclose a driving method that comprises the step of (a) generating a signal having a frequency, (b) detecting the phase difference between the horizontal synchronizing signal and the generated signal by comparing these signals, (c) integrating the compare signals to generate a detected signal, (d) adjusting the frequency of the reference signal in response to the detected signal, and (d) providing a driving signal to a light source (see e.g. col. 6, lines 24-38; col. 7, lines 1-12; fig. 1).

The teachings of Tanaka et al. differs from the presently claimed invention as follows:

For ***claim 1 and 15***, the device of Tanaka et al. fails to include a controller that modulate the reference signal in response to the control signal and output a modulated signal such that the modulation is a pulse width modulation.

For ***claims 4 and 5***, although Tanaka et al. fail to disclose that the circuit of the phase comparator include logic gate, it is art recognized that the circuit of the phase comparator include logic gate such as XOR as evidence by Okamoto (US patent 6,944,252 B2; *filing date of 09/21/2001*)(see e.g. col. 1, line 23 and 35-38; fig. 12, ref. #12). Furthermore, the type of logic gate, i.e. XOR or XNOR, use would be would be a choice of experimental design and is considered within the purview of the cited prior art.

For ***claims 9 and 10***, the device of Tanaka et al. fails to include a frequency divider that divide a frequency of the modulated signal provided from the controller to generate a frequency-divided signal such that the frequency of the modulated signal is twice a frequency of the frequency-divided signal.

For ***claim 11***, the device of Tanaka et al. fails to include a low pass filter that filter out high frequency components of the output signal of the phase comparator.

For ***claim 12***, the device of Tanaka et al. fails to include a switch circuit that receive the modulated signal from the controller and generate a switch signal having on and off levels by switching a supply voltage in accordance with the modulated signal.

For ***claim 20***, Tanaka et al. fail to disclose the step of (a) performing pulse width modulation with respect to the reference signal to generate a modulated signal, and (b) dividing a frequency of the modulated signal to generate a frequency-divided signal.

For ***claim 21***, Tanaka et al. fail to disclose the step of filtering out high frequency components of the result signal obtained from the comparing step.

However, Jefferson teaches the limitations that are deficient in Tanaka et al.

Jefferson discloses a logic device that includes a PLL system (ref. #62 of fig. 3)(see e.g. col. 5, line 41 thru col. 7, line 11). The PLL system as illustrated by figure 3 includes a phase frequency detector (ref. #68 of fig. 3), a low pass filter (ref. #70 of fig. 3), a voltage control oscillator (ref. #66 of fig. 3), a delay element (ref. #72 of fig. 3), a divide-by-two circuit (ref. #74 of fig. 3), and a multiplexer (ref. #75 of fig. 3)(see e.g. col. 5, line 61 thru col. 7, line 11).

For ***claim 1, 15, and 20***, Jefferson discloses that the delay element (refers to instant claimed controller) receive the clock signal (refers to instant claimed reference signal) from the voltage control oscillator and modulate it in response to the reference clock signal (refers to instant claimed control signal) to produce an output signal (see e.g. col. 6, line 55 thru col. 7, line 11; fig. 3).

For ***claims 9, 10, 20, and 21***, Jefferson discloses that the divide-by-two circuit (refers to instant claimed frequency divider) divides the output signal from the delay element to produce a frequency- divided signal such that the frequency of the modulated signal is twice a frequency of the frequency-divided signal (see e.g. col. 5, lines 64-65; col. 8, lines 44-53).

For ***claim 11***, Jefferson discloses that the low pass filter is to filter out higher frequency components from the phase frequency detector (refers to instant claimed phase comparator), and it is placed after the phase frequency detector (see e.g. col. 6, lines 34-40; fig. 3).

For ***claim 12***, Jefferson discloses that the multiplexer (refers to instant claimed switch circuit) receive the output signal from the delay element to generate a switch signal having on

and off levels by switching a supply voltage in accordance with the output signal (see e.g. col. 5, lines 65-67; fig. 3).

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to disclose the limitations of claims 1, 9-12, 15, 20, and 21 as discussed above that is taught by Jefferson in the device of Tanaka et al. One of ordinary skill in the art would have been motivated to disclose the limitations of claims 1, 9-12, 15, 20, and 21 as discussed above in the device of Tanaka et al. for the advantage of providing a device that can receive two different phase shift signals (Jefferson: col. 3, lines 35-41). Furthermore, one of ordinary skill in the art would have a reasonable expectation of success in the combination of Tanaka et al. and Jefferson because the PLL system of both Tanaka et al. and Jefferson is use to produce a clock signal from two different phase shift signals.

Therefore, the combine teachings of Tanaka et al. and Jefferson do render the apparatus and method of the instant claims *prima facie* obvious.

Allowable Subject Matter

10. Claims 6-8, 13, 14, and 19 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

11. The following is a statement of reasons for the indication of allowable subject matter:

A. The instant claims 6 and 13 are allowed for the reason that the cited prior arts do not teach or fairly suggest the presently claimed device wherein the integrator includes an

operational amplifier, and '*a transformer to receive the switch signal from the switch circuit and generate a sinusoidal signal which is applied to the light source*'.

B. The instant claim 19 is allowed for the reason that the cited prior arts do not teach or fairly suggest the presently claimed method with the step of '*resetting the integrating step such that the integrated voltage signal returns to an initial status*'.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to MY-CHAU T. TRAN whose telephone number is 571-272-0810. The examiner can normally be reached on Monday: 8:00-2:30; Tuesday-Thursday: 7:30-5:00; Friday: 8:00-3:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard A. Hjerpe can be reached on 571-272-7691. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

My-Chau T. Tran
January 18, 2007

RICHARD HJERPE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600